REMARKS

The following remarks are submitted in light of the Office Action mailed January 9, 2006. Claim 1-16 are presented for examination of which Claim 1 is the only independent claim. No new matter has been added.

Rejection of Claims 1-8 and 10-12 under 35 U.S.C. §102(b) as being anticipated by Japan Patent No. 5-335482 to Yamazaki et al ("Yamazaki").

Claims 1-8 and 10-12 are rejected under 35 U.S.C. §102(b) as being anticipated by Japan Patent No. 5-335482 to Yamazaki et al. ("Yamazaki"). Applicants respectfully traverse this rejection.

Claim 1 is directed to a semiconductor wafer. The semiconductor wafer of Claim 1 comprises a substrate, a plurality of integrated circuit chips, a dicing channel disposed between adjacent ones of integrated circuit chips, the channel exposing sidewalls of the integrated circuit chips, and a layer of first dielectric material disposed on a top surface and sidewalls of the integrated circuit chips. Thus, it is a feature of the invention that a dicing channel exposes the sidewalls of the integrated circuit chips. It is a further feature of the invention that a layer of first dielectric material is disposed on a top surface and sidewalls of the integrated circuit chips.

While the claimed invention is directed to a semiconductor wafer, Yamazaki, on the other hand, is directed to an integrated circuit. The integrated circuit in Yamazaki, as depicted in Figure 3, is contained on a substrate such as a semiconductor wafer or glass plate. Yamazaki is directed to an integrated circuit, and more specifically, an integrated circuit with multiple layers. Figures 1-2 in Yamazaki depict a cross section of the integrated circuit with multiple layers exploded from the semiconductor wafer depicted in Figure 3.

Yamazaki fails to disclose a dicing channel that exposes the sidewalls of the integrated circuit chips as required by the claimed invention. Additionally, Yamazaki fails to disclose a first dielectric material disposed on the top surface and sidewalls of the integrated circuit chips as required by the claimed invention. Since Yamazaki fails to disclose each and every element of the claimed invention, Applicants respectfully

submit that Claim 1 is not anticipated by Yamazaki. Claims 2-8 and 10-12 depend from claim 1, and by virtue of their dependence on an allowable base claim are not anticipated by Yamazaki and are similarly allowable.

Applicants respectfully traverse the Examiner's analysis of Yamazaki. The Examiner points to reference numeral 16 in Figure 2 of Yamazaki for disclosure of the claimed dicing channel, however as stated in the abstract reference numeral 16 in Figure 2 depicts wiring, and not a dicing channel. More specifically, as stated in the abstract reference numeral 16 in Figure 2 depicts an aluminum film wiring. Even were reference number 16 in Yamazaki a dicing channel, Yamazaki fails to disclose a dicing channel exposing sidewalls of integrated circuit chips as required by Claim 1. As stated in the title Yamazaki is a "Multilayer Semiconductor Integrated Circuit Film Resistor." Figure 3 in Yamazaki depicts where this integrated circuit resides, namely on a semiconductor wafer, while Figure 1 in Yamazaki depicts the integrated circuit exploded from the Figure 3 view, and Figures 2(A)-2(F) depict the construction of the integrated circuit depicted in Figure 1. Not only does Yamazaki not disclose a dicing channel that exposes the sidewalls of an integrated circuit as required by Claim 1, but also Yamazaki does not disclose a layer of first dielectric material disposed on the top surface and sidewalls of the integrated circuit chips as further required by Claim 1.

Yamazaki fails to disclose each feature of Claim 1, therefore, Yamazaki does not anticipate Claim 1. Claims 2-8 and 10-12 depend from Claim 1, and therefore Yamazaki also does not anticipate Claims 2-8 and 10-12 by virtue of their dependence on allowable Claim 1. For at least these reasons, Applicants respectfully request withdrawal of the 35 U.S.C. §102(b) rejection applied against Claims 1-8 and 10-12.

Rejection of Claims 13-16 under 35 U.S.C. §103(a) as being unpatentable over Yamazaki

Claims 13-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki. Applicants respectfully traverse this rejection.

Claims 13-16 depend from Claim 1. As discussed previously, it is a feature of the invention that a dicing channel exposes the sidewalls of the integrated circuit chips.

It is a further feature of the invention that a layer of first dielectric material is disposed on a top surface and sidewalls of the integrated circuit chips.

Not only does Yamazaki fail to disclose, teach, or suggest either a dicing channel that exposes the sidewalls of the integrated circuit chips or a layer of first dielectric material disposed on the top surface and sidewalls of the integrated circuit chips, but also Yamazaki fails to recognize the importance of such the dicing channel and layer of first dielectric material.

Therefore, Applicants respectfully submit that Claim 1 is patentable over Yamazaki. Claims 13-16 depend from Claim 1, and therefore Yamazaki also does not anticipate Claims 13-16 by virtue of their dependence on allowable Claim 1. For at least the foregoing reasons, Applicants respectfully request withdrawal of the 35 U.S.C. §103(a) rejection applied against Claims 13-16.

Rejection of Claim 9 under 35 U.S.C. §103(a) as being unpatentable over Yamazaki in view of U.S. Patent Application Publication 2003/0222330 A1 to Sun et al.

Claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki in view of U.S. Patent Application Publication 2003/0222330 A1 to Sun et al. ("Sun"). Applicants respectfully traverse this rejection.

Claim 9 depends from Claim 1. As discussed previously, it is a feature of the invention that a dicing channel exposes the sidewalls of the integrated circuit chips. It is a further feature of the invention that a layer of first dielectric material is disposed on a top surface and sidewalls of the integrated circuit chips. Applicants respectfully submit that these features are neither disclosed nor suggested by the combination of Yamazaki and Sun.

Sun fails to compensate for the deficiencies of Yamazaki. As stated in the title Sun is directed to "Passivation Processing over a Memory Link." Sun fails to disclose a dicing channel that exposes the sidewalls of integrated circuit chips as required by Claim 1. Sun also fails to disclose a layer of first dielectric material disposed on a top surface and sidewalls of the integrated circuit chips as further required by Claim 1. For

at least these reasons, the claimed invention is patentable over the combination of Yamazaki and Sun.

Therefore, Applicants respectfully submit that Claim 1 is patentable over the combination of Yamazaki and Sun. Claim 9 depends from Claim 1, and therefore Claim 9 by virtue of its dependence on allowable Claim 1 is also patentable over the combination of Yamazaki and Sun. For at least the foregoing reasons, Applicants respectfully request withdrawal of the 35 U.S.C. §103(a) rejection applied against Claim 9.

Conclusion

Applicants have properly traversed each of the grounds for rejection in the Office Action, and therefore respectfully submit that the application is in condition for allowance. Reconsideration and allowance of pending claims is respectfully requested.

If the Examiner has any questions or believes further discussion will aid examination and advance prosecution of the application, a telephone call to the undersigned is invited.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, the Commissioner is authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully Submitted,

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